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531 Rec'd PCT/PT 15 JAN 2002

U.S. APPLICATION NO. <b>10/031058</b> INTERNATIONAL APPLICATION NO. PCT/DE00/02296		ATTORNEY'S DOCKET NUMBER 8074-7 (S1656 GC/rfu)	
21. <input type="checkbox"/> The following fees are submitted: <b>BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):</b> Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO ..... <b>\$1040.00</b> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO ..... <b>\$890.00</b> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO ..... <b>\$740.00</b> International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) ..... <b>\$710.00</b> International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) ..... <b>\$100.00</b> <b>ENTER APPROPRIATE BASIC FEE AMOUNT =</b>		<b>CALCULATIONS PTO USE ONLY</b>	
Surcharge of <b>\$130.00</b> for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input checked="" type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).		\$ 890.00 \$ 130.00	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE
Total claims	5 - 20 =	0	x \$18.00
Independent claims	1 - 3 =	0	x \$84.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ \$280.00
<b>TOTAL OF ABOVE CALCULATIONS =</b>		\$	
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.		\$ 0	
<b>SUBTOTAL =</b>		\$	
Processing fee of <b>\$130.00</b> for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(f)).		\$ 0	
<b>TOTAL NATIONAL FEE =</b>		\$ 1,020.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). <b>\$40.00</b> per property +		\$ 0	
<b>TOTAL FEES ENCLOSED =</b>		\$ 1,020.00	
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a. <input checked="" type="checkbox"/> A check in the amount of \$ <u>1,020.00</u> to cover the above fees is enclosed. b. <input type="checkbox"/> Please charge my Deposit Account No. _____ in the amount of \$ _____ to cover the above fees. A duplicate copy of this sheet is enclosed. c. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. <u>50-0679</u> . A duplicate copy of this sheet is enclosed. d. <input type="checkbox"/> Fees are to be charged to a credit card. <b>WARNING:</b> Information on this form may become public. <b>Credit card          information should not be included on this form.</b> Provide credit card information and authorization on PTO-2038.			
<b>NOTE:</b> Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.			
SEND ALL CORRESPONDENCE TO: Frank Chau F. Chau & Associates, LLP 1900 Hempstead Turnpike, Suite 501 East Meadow, New York 11554 (516) 357-0091			
		 SIGNATURE Frank V. DeRosa NAME 43,584 REGISTRATION NUMBER	

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**PATENT APPLICATION**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Applicants:** Christian Panis, Christian Schranz, Herbert Zojer, Manfred Preitnegger

**International Application No.:** PCT/DE00/02296

**International Filing Date:** 13 July 2000

**Priority Date Claimed:** 15 July 1999

**U.S. Serial No.:** unassigned

**Group Art Unit:** unassigned

**Docket:** 8074-7 (S1656 GC/rfu)

**FOR: BROADBAND NETWORK ACCESS DEVICE FOR THE  
TRANSMISSION OF VOICE AND DATA**

Assistant Commissioner for Patents  
BOX PCT  
Washington, D.C. 20231

**PRELIMINARY AMENDMENT**

Prior to examination on the merits of the above-identified International Application in the United States National Phase, please amend the above-identified application as follows:

**CERTIFICATE OF MAILING 37 C.F.R. § 1.10**

I hereby certify that this Preliminary Amendment is being deposited with the United States Postal Service on this date of January 15, 2002 in an envelope as "Express Mail Post Office to Addressee" Mail Label Number **EL922712206US** addressed to "Assistant Commissioner for Patents, BOX PCT, Washington, D.C. 20231."

Date: 4/15/02

Frank V. Derosa

FRANK V. DEROSA

**IN THE CLAIMS:**

Please cancel claims 1-9 as originally filed in the International Application without prejudice.

Please add the following New claims:

10. (New) A broadband network access device for the transmission of voice and data, comprising:

one or more broadband subscriber line interface circuits, parallel with one another, for connecting to analog telephone subscriber lines;

a splitting device which splits narrowband, low-frequency voice signals and broadband, higher-frequency data signals from one another in both directions of transmission and converts the voice and data signals into a digital signal in the direction of transmission to a network by sampling, and in the opposite direction of transmission into an analog signal;

a digital voice signal processor for processing the voice signal data, which is connected to a digital voice network;

a digital data signal processor for processing the data signal data, which is connected to a digital data network;

wherein the voice signals are sampled in the splitting device in the direction of transmission to the digital voice network with a multiple of a data clock base, and subsequently decimated, and the data, decimated to the voice clock, is transmitted to the digital voice signal processor in a data clock pattern which is multiple of the data clock base; and

wherein the conversion to a voice data pattern, which is a multiple of a voice clock base, is carried out in a synchronization interface module upstream of the digital voice signal processor which is provided for processing the voice data; and

a phase locked loop that is supplied with a multiple of the voice clock base and generates a signal with a frequency that is a multiple of the data clock base on which the data sampling is based.

11. (New) The broadband network access device of claim 10, wherein the synchronization module is combined at the module level with the digital voice signal processor that is provided for processing the voice data.

12. (New) The broadband network access device of claim 10, wherein the synchronization interface module is embodied as a device for performing soft synchronization between the data clock pattern and the voice data pattern.

13. (New) The broadband network access device of claim 10, wherein the data clock base is 4.3125 kHz and the voice clock base is 8 kHz.

14. (New) The broadband network access device of claim 10, wherein the broadband network access device is used for implementing a xDSL (x-Digital Subscriber Line) system.

#### REMARKS

Entry of this Preliminary Amendment prior to the examination of the above-identified International Application, United States National Phase, on the merits is respectfully requested. No new matter has been added by the Preliminary Amendment. Early and favorable consideration of this application is requested.

Respectfully submitted,



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# Description

Broadband network access device for the transmission of voice and data

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The invention relates to a broadband network access device for the transmission of voice and data, having one or more broadband subscriber line interface circuits, parallel with one another, for connecting to analog telephone subscriber lines, having a device which splits narrowband, low-frequency voice signals and broadband, higher-frequency data signals in both directions of transmission and which also converts the voice and data signals into the digital form in the direction of the network by sampling and into the analog form in the opposite direction, and having a digital signal processor which is provided for processing the voice signal data and which is connected to a digital voice network, and a digital signal processor which is provided for processing the data signal data and is connected to a digital data network.

The transmission of voice via an analog subscriber line in a telephone network is carried out in analog form. It is done using a frequency band, what is referred to as the voice band, which constitutes only a relatively narrow frequency band of the entire transmission bandwidth of a copper double conductor (POTS = Plain Old Telephone System). In what are referred to as xDSL (x-Digital Subscriber Line) transmission methods, the frequency ranges above the voice band are also used for data transmission in a broadband fashion in a telephone network. xDSL transmission methods include HDSL (High Bit Rate Digital Subscriber Line), ADSL (Asymmetric Digital Subscriber Line) and VDSL (Very High Speed Digital Subscriber Line). The xDSL transmission methods are referred to as broadband network access technology and comprise all the transmission methods via the

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telephone network which make possible a higher data transmission rate between a subscriber and the central office (CO) than the data transmission rate which can be achieved with voice band modems. To do this, in the  
5 xDSL transmission methods, what is referred to as an xDSL data signal, which designates a digital signal which is encoded for the xDSL transmission method, is transmitted in a higher frequency band, the data band, which is separated from the voice band. The xDSL  
10 transmission methods can theoretically use the entire bandwidth of the copper double conductor available above the voice band and achieve data transmission rates in the Mbit/s range.

15 When designing a broadband network access device for such a voice signal/data signal transmission method it is to be noted that the clock pattern which is customary for the transmission of voice is normally based on multiples of the voice bandwidth of 4 kHz,  
20 which gives rise to a data clock base of 8 kHz. The latter is not suitable for the transmission of data because in the DMT method used here the sampling rate is obtained as a multiple of the distance between two subcarriers of 4.3125 kHz, which is referred to below  
25 as the data clock base.

The invention is based on the object of constructing and operating a common broadband network access device for the transmission of voice and data in such a way  
30 that the sampling rates and clock systems which are predefined for the data transmission range and the voice transmission range are combined in a fully operationally capable fashion.

35 According to the invention, which relates to a broadband network access device for the transmission of voice and data of the type mentioned at the beginning, this object is achieved in that the voice signals are sampled in the direction of transmission to the voice

network with a multiple of the data clock base and are subsequently decimated, in that the data which has already been decimated to the voice clock is still transmitted in the data clock pattern to the digital signal processor provided for processing the voice signals, in that the conversion to the voice data pattern is carried out in a synchronization interface module directly upstream of the digital signal processor which is provided for processing the voice data, and in that the sampling in the opposite direction of transmission takes place in a functionally corresponding fashion. The specified measures successfully combine the two different sampling rates or clock systems, the user very easily obtaining synchronization between his data path and his voice path and a complex, external synchronization process thus being avoided.

20 The synchronization interface module is expediently combined at the module level with the actual digital signal processor which is provided for processing the voice data.

25 In the broadband network access device according to the invention, the synchronization interface module is expediently embodied as a device for performing soft synchronization between the data clock pattern and the voice data pattern.

30 The broadband network access device according to the invention can advantageously be used for implementing an xDSL (x-Digital Subscriber Line) system, for example an ADSL (Asymmetric Digital Subscriber Line) system.

35 The broadband network access device according to the invention is particularly expediently embodied using integrated circuit technology. With such technology, inter alia, the device which splits the voice and data signals in both directions of transmission and which





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bidirectionally effective fashion to a device B-QAP (Broadband-Quad Analog POTS), which splits the narrowband, low-frequency voice signals and the broadband, higher-frequency data signals in both  
5 directions of transmission and, integrated in this way, converts the voice and data signals into digital signals in the one direction of transmission and into analog signals in the opposite direction of transmission.

10

The digitized and decimated voice signal is then fed to a digital signal processor B-MUPP (Broadband Multichannel Processor for POTS) for processing voice signals, while the digitized data  
15 signal is fed via data lines DDU-0 (DDU = Digital Data Upstream) and DDU-1 to two digital signal processors DSP-0 and DSP-1 which are configured, through cooperation, as a data pump for processing digital signals. The voice data which is processed in the  
20 digital signal processor B-MUPP is then input, for example in PCM form, into a correspondingly configured, digital voice network.

In a similar way, the data signals which are processed  
25 in the two digital signal processors DSP-0 and DSP-1 are then fed, for example as ATM signals, into a correspondingly configured, digital data network. The digital voice network and the digital data network connect corresponding central offices to one another.  
30 In the opposite direction of transmission, the digital signal processor B-MuPP and the two digital signal processors DSP-0 and DSP-1 receive a digital voice signal and a digital data signal from the digital voice network and from the digital data network,  
35 respectively.

The digital voice signal which is received from the digital voice network is fed to the device B-QAP by the digital voice signal processor B-MuPP. The digital data

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signal which is received from the digital data network is fed by the digital data signal processor DSP-0 and DSP-1, via the data lines DDD-0 and DDD-1 (DDD = Digital Data Downstream), to the device B-QAP which converts all the digital signals in this direction of transmission into analog signals and in which the narrowband, low-frequency voice signal and the broadband, higher-frequency data signal are also combined to form an analog composite signal, which is fed to the subscribers via the subscriber line interface circuits and the subscriber lines.

The connection to the voice network is established via an IOM/PCM interface IOM/PCM. At said voice network, the sampling frequency is 4.096 MHz. Using a phase locked loop PLL which is equipped with a quartz-stabilized oscillator VCXO or DCXO and which is supplied with the sampling frequency of 4.096 MHz of the IOM/PCM voice network, a frequency of 35.328 MHz is generated, which is a multiple (8192 times) of the data clock base of 4.3125 kHz on which the data sampling is based according to standard practice.

The device B-QAP, the digital signal processor B-MuPP which is responsible for voice and the two digital signal processors DSP-0 and DSP-1 which are responsible for the data are supplied with this frequency of 35.328 MHz. Between the device B-QAP and the two digital signal processors DSP-0 and DSP-1 there are dedicated data interfaces via the data lines DDU-0/DDD-0 and DDU-1/DDD-1.

The synchronization of the two digital signal processors DSP-0 and DSP-1 for the processing and transmission of the digital data signals is carried out via the line DFSC (Data Frame Synchronization). Control information is also necessary for the sequence control of the sampling in the device B-QAP. For this purpose, an interface is defined between the sampling device

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B-QAP and the digital signal processor B-MuPP which is responsible for the voice signal processing.

5 This interface, which is also contained in the circuit module which contains the actual digital signal processor B-MuPP, is used both for transmitting control and check data (AFSC = Analog Frame Synchronization) and the voice signal itself. As FIG. 2 shows, the voice data is sampled in the device B-QAP with 17.664 MHz,  
10 that is to say with a multiple (4096 times) of the data clock base of 4.3125 kHz and subsequently decimated.

The transmission of the voice data, already decimated to the voice clock, to the digital voice signal  
15 processor B-MuPP is still carried out in the data clock pattern, that is to say at 17.664 MHz. The conversion to the voice pattern of 16.384 MHz, on which the voice basic sampling frequency of 8 kHz is based and which is a multiple (2048 times) of this voice basic sampling  
20 frequency, takes place in an interface in an interface module SM, which is located in the voice signal processor module B-MuPP, connected directly upstream of the actual digital voice signal processor DSP. The synchronization interface module SM is embodied as a  
25 device for soft synchronization (soft synchro) between the data clock pattern and the voice data pattern. The sampling in the opposite direction of transmission is carried out in a functionally corresponding fashion.

30 The broadband network access device illustrated in FIG. 1 and 2 is embodied using integrated circuit technology, specifically in one chip set. This chip set contains, inter alia, the device B-QAP which splits the voice and data signals in both directions of  
35 transmission and in which, however, the voice and data signals are also converted into the digital form in the direction of the network by sampling, and in the opposite direction into the analog form.

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- Furthermore, the chip set includes the digital signal processor B-MuPP which processes the digital voice signals, including the interface module SM, the digital signal processors DSP-0, DSP-1 which process the
- 5 digital data signals and the phase locked loop PLL which is provided for generating the clock and has a quartz-stabilized, controlled oscillator, each of these in the form of integrated circuit modules.
- 10 In the embodiment of a broadband network access device described with reference to FIG. 1 and 2, the user very easily obtains synchronization between his data path and his signal path, and a complex, external synchronization process is avoided.

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## Patent Claims

1. A broadband network access device for the transmission of voice and data, having one or more  
5 broadband subscriber line interface circuits, parallel with one another, for connecting to analog telephone subscriber lines, having a device which splits narrowband, low-frequency voice signals and broadband, higher-frequency data  
10 signals in both directions of transmission and which also converts the voice and data signals into the digital form in the direction of the network by sampling, and into the analog form in the opposite direction, and having a digital  
15 signal processor which is provided for processing the voice signal data and which is connected to a digital voice network, and a digital signal processor which is provided for processing the data signal data and is connected to a digital  
20 data network, wherein the voice signals are sampled in the direction of transmission to the voice network with a multiple of the data clock base and are subsequently decimated, wherein the data which has already been decimated to the voice  
25 clock is still transmitted in the data clock pattern to the digital signal processor (B-MuPP) provided for processing the voice signals, wherein the conversion to the voice data pattern is carried out in a synchronization interface module  
30 (SM) directly upstream of the actual digital signal processor (DSP) which is provided for processing the voice data, and wherein the sampling in the opposite direction of transmission takes place in a functionally corresponding way.  
35
2. The broadband network access device as claimed in claim 1, wherein the synchronization interface module (SM) is combined at the module level with

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the actual digital signal processor (DSP) which is provided for processing the voice data.

- 5 3. The broadband network access device as claimed in claim 1 or 2, wherein the synchronization interface module (SM) is embodied as a device for performing soft synchronization between the data clock pattern and the voice data pattern.
- 10 4. The broadband network access device as claimed in one of the preceding claims, distinguished by a data signal sampling rate which is a multiple of 4.3125 kHz (= data clock base) and a voice signal sampling rate which is a multiple of 8 kHz  
15 (= voice clock base).
5. The broadband network access device as claimed in one of the preceding claims, characterized by a use for implementing an xDSL  
20 (x-Digital Subscriber Line) system, for example an ADSL (Asymmetric Digital Subscriber Line) system.
6. The broadband network access device as claimed in one of the preceding claims, characterized by an  
25 embodiment in integrated circuit technology.
7. The broadband network access device as claimed in claim 7, wherein, inter alia, the device (B-QAP) which splits the voice and data signals in both  
30 directions of transmission and which also converts the voice and data signals in the direction of the network by sampling in a digital form and in an analog form in the opposite direction, the digital signal processor (B-MuPP) which processes the  
35 digital voice signals, including the interface module (SM), the digital signal processor (DSP-0) which processes the digital data signals, and a phase locked loop (PLL) which is provided for generating the clock and has a quartz-stabilized,

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controlled oscillator are each formed by a separate integrated circuit module in one chip set.

5 8. The broadband network access device as claimed in one of the preceding claims, wherein the digital signal processors (DSP, DSP-0, DSP-1) are each composed - depending on the size requirements - of a plurality of subunits which can each be  
10 integrated at the module level.

9. The broadband network access device as claimed in claim 7, wherein the phase locked loop (PLL) which is provided for generating the clock and is  
15 equipped with a quartz-stabilized, controlled oscillator is combined with the digital signal processor (B-MuPP) which processes the digital voice signals, in a single integrated circuit module.



## Abstract

Broadband network access device for the transmission of voice and data

In the broadband network access device for transmitting narrowband, low-frequency voice signals and broadband, higher-frequency data signals, the voice data is sampled in the data clock pattern and subsequently decimated. The transmission of the data which has already been decimated to the voice clock to the voice DSP (DSP) is still carried out in the data clock pattern. The conversion to the voice clock pattern is carried out in a synchronization interface (SM), directly upstream of the voice DSP. The same applies correspondingly in the opposite direction of transmission. The invention is used in xDSL methods, for example ADSL.Lite.

FIG. 2

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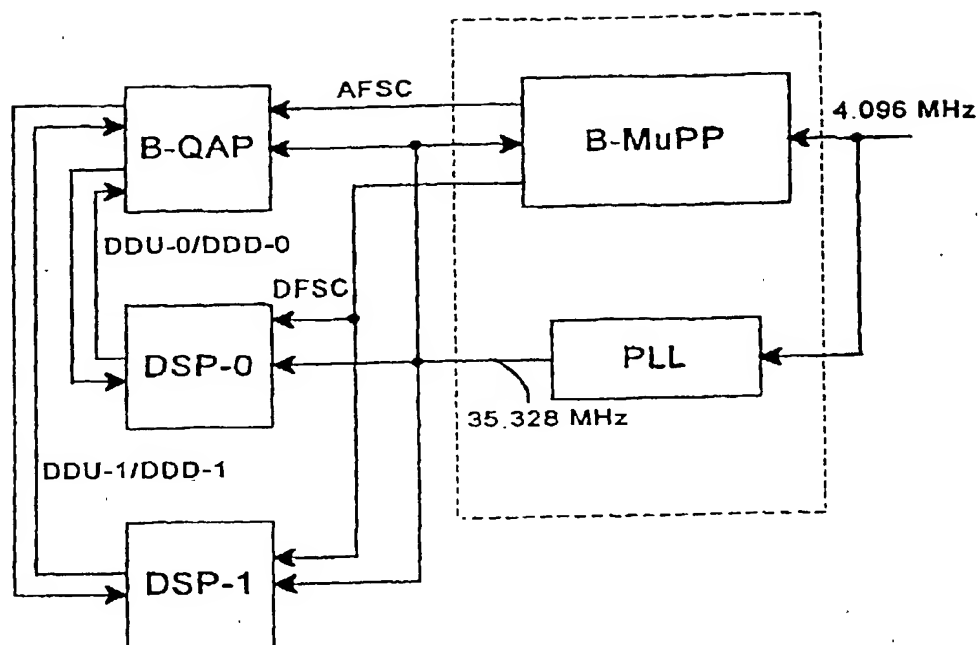


FIG. 1

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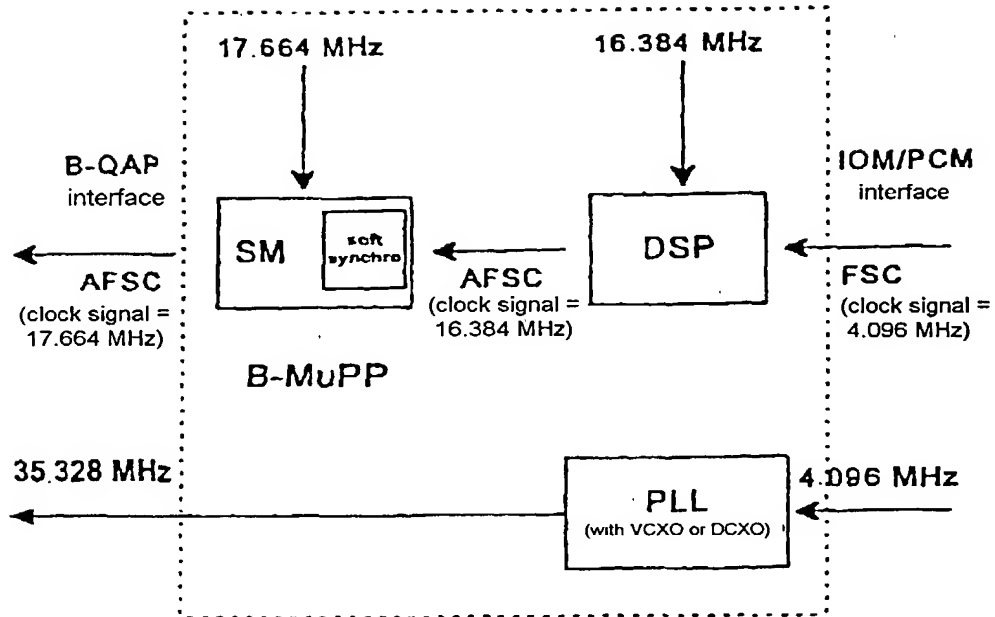


FIG. 2

My residence, post office address and citizenship are as stated next to my name.

**TITLE: BROADBAND NETWORK ACCESS DEVICE FOR THE TRANSMISSION OF VOICE AND DATA**

the specification of which either is attached hereto or indicates an attorney Docket No. 8074-7 (S1656 GC/rfu), or

☒ was filed in the U.S. Patent & Trademark Office on January 15, 2002 and assigned Serial No. 10/031,058,

☐ and (if applicable) was amended on

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability and to the examination of this application in accordance with Title 37 of the Code of Federal Regulations '1.56.

I hereby claim foreign priority benefits under Title 35, U.S. Code '119(a)-(d) or '365(b) of any foreign application(s) for patent or inventor's certificate, or '365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below any foreign applications for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

19933264.9	Germany	15 July 2001	<b>Priority Claimed:</b> Yes [X] No [ ]
<i>(Application Number)</i>	<i>(Country)</i>	<i>(Day/Month/Year filed)</i>	
			Yes [ ] No [ ]
<i>(Application Number)</i>	<i>(Country)</i>	<i>(Day/Month/Year filed)</i>	

I hereby claim the benefit under Title 35, U.S. Code, '120 of any United States application(s), or '119(e) of any United States provisional application(s), or '365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of Title 35, U.S. Code, '112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, The Code of Federal Regulations, '1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

PCT/DE00/02296	13 July 2000	Pending
(Application Serial Number)	(Filing Date)	(STATUS: patented, pending, abandoned)
(Application Serial Number)	(Filing Date)	(STATUS: patented, pending, abandoned)

I hereby appoint the following attorneys: **FRANK CHAU**, Reg. No. 34,136; **FRANK V. DeROSA**, Reg. No. 43,584; **JUAN C. VILLAR**, Reg. No. 34,271; **NATHANIEL T. WALLACE**, Reg. No. 48,909; **ERIC M. PARHAM**, Reg. No. 45,747; and **GEORGE D. MORGAN**, Reg. No. 46,505; each of them of **F. CHAU & ASSOCIATES, LLP**, 1900 Hempstead Turnpike, Suite 501, East Meadow, New York 11554 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith and with any divisional, continuation, continuation-in-part, reissue or re-examination application, with full power of appointment and with full power to substitute an associate attorney or agent, and to receive all patents which may issue thereon, and request that all correspondence be addressed to:

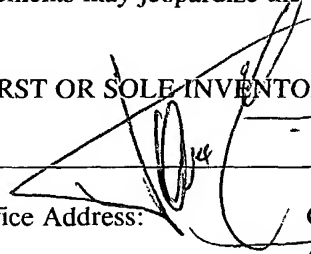
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301131058, 06.3.112

I HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under '1001 of Title 18 U.S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1-00  
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Inventor's signature: 

Date: 6.4.02

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2-00  
FULL NAME OF SECOND INVENTOR: Christian SCHRANZ

Citizenship AUSTRIA

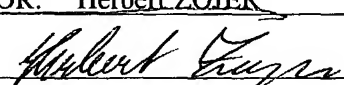
Inventor's signature: 

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3-00  
FULL NAME OF THIRD INVENTOR: Herbert ZOIER

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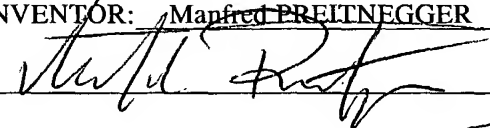
Inventor's signature: 

Date: 02.05.02

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4-00  
FULL NAME OF FOURTH INVENTOR: Manfred PREITNEGGER

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Inventor's signature: 

Date: 11.4.02

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